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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUR, JUNG H	

ART UNIT	PAPER NUMBER
2824	

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02/11/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/757,259	BUER ET AL.	
	Examiner	Art Unit	
	J. H. Hur	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-10,13-17 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4-10,13-17 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *14 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09 January 2008 has been entered.

Amendment

2. Acknowledgment is made of applicant's Amendment, filed 09 January 2008. The changes and remarks disclosed therein have been considered.

No claims have been cancelled or added by Amendment. Therefore, claims 1, 4-10, 13-17 and 20 remain pending in the application.

Specification

3. Claim 8 is objected to because of the following informalities:

In claim 8, being dependent on claim 1, "if the states" should be --if states--, and "is equal to a first and second expected states" as --are respectively equal to first and second expected states--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 4-6, 8-10, 13, 14 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. Pat. No. 5,996,091) in view of Gelsomini et al. (U.S. Pat. No. 6,611,040).

Regarding claim 1, Jones, for example in Figs. 3a and 3b, discloses a method of verifying a state of an element (for example, an element of memory 304 in Fig. 3a corresponding to DR0 in Fig. 3b) comprising: determining if the state of the element (DR0 in Fig. 3b) is equal to an expected state (VERIFY DATA 0 in Fig. 3b) using a verify circuit (308 in Fig. 3a); and outputting a valid signal (FAST VERIFY OUTPUT of 390 in Fig. 3b) if the state of the element is equal to said expected state (if DR0 is equal to VERIFY DATA 0 in Fig. 3b; see also column 4, lines 21-27).

Jones also implies that fuses (or anti-fuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in Jones (see for example column 13, lines 23-26).

Jones does not disclose that the state of the element is a state of the electrical resistance of the element and that the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick.

Gelsomini discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6

and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent, as a fuse).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute a thin oxide gated fuse having an oxide that is less than 2.5nm thick for the memory element of Jones, as an equivalent memory element, with an optimum oxide thickness, such that the state of the element is a state of the electrical resistance of the element, for the purpose of minimizing the voltage and duration of a programming pulse (as implied in Gelsomini, column 4, lines 2-6), since discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art.

Regarding claims 4-6 and 8, the above combination further discloses sensing the state of the element (to store in DATA SHIFT REGISTER 310 in Fig. 3b of Jones; see also sense amplifiers S/A 132 in Fig. 1 of Gelsomini);

generating a high signal if the state of the element is equal to said expected state (the output of 390 in Fig. 3b of Jones; see also column 4, lines 21-27);

generating a low signal if the state of the element is not equal to said expected state (the output of 390 in Fig. 3b of Jones; see also column 4, lines 21-27);

wherein outputting a valid signal includes determining if states of both first and second thin oxide gated fuses (for example, DR0 and DR9 in Fig. 3b of Jones) are respectively equal to first and second expected states (for example, VERIFY DATA 0 and VERIFY DATA 9).

Regarding claim 9, Jones, for example in Figs. 3a and 3b, discloses a method for verifying a state of a memory device (304 in Fig. 3a) comprising: comparing a state of a first element (corresponding to DR0 in Fig. 3b) to a first expected state (VERIFY DATA 0 in Fig. 3b), and generating a first signal (output of 380); comparing a state of a second element (corresponding to DR9 in Fig. 3b) to a second expected state (VERIFY DATA 9 in Fig. 3b), and generating a second signal (output of 389); and outputting a valid signal (FAST VERIFY OUTPUT of 390) if both said first and second signals are the same (the XNOR function of 390).

Jones also implies that fuses (or anti-fuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in Jones (see for example column 13, lines 23-26).

Jones does not disclose that the first and second elements are thin oxide gated fuses having an oxide that is less than 2.5nm thick, and that the state is a state of the electrical resistance.

Gelsomini discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent, as a fuse).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute a thin oxide gated fuse having an oxide that is less than 2.5nm thick for the first and second memory elements of Jones, as an equivalent memory element, with an optimum oxide thickness, such that the state is a state of the electrical resistance, for the purpose of minimizing the voltage and duration of a programming pulse (as

implied in Gelsomini, column 4, lines 2-6), since discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art.

Regarding claim 10, the above combination discloses the method of claim 9, with the exception of outputting a valid signal if both said first and second signals are high. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to output a valid signal if both said first and second signals are high (and modify accordingly the comparison logic of Fig. 3B of Jones; also compare, for example, Figs. 16a and 18a), since such designation of a logic state to indicate the result of a condition requires only routine skill in the art.

Regarding claims 13 and 14, the above combination further discloses determining if said state of said first thin oxide gated fuse is equal to said first expected state (via 380 in Fig. 3b of Jones), and determining if said state of said second thin oxide gated fuse is equal to said second expected state (via 389 in Fig. 3b of Jones).

Regarding claim 17, Jones, for example in Figs. 3a and 3b, discloses a method for verifying a state of a memory device (304 in Fig. 3a), comprising: setting a first expected state (VERIFY DATA 0 in Fig. 3b); sensing a state of a first element (to store in DATA SHIFT REGISTER 310); determining if said state of said first element (DR0) is equal to said first expected state (via 380) and generating a first signal (output of 380); setting a second expected state (VERIFY DATA 9 in Fig. 3b); sensing a state of a second element (to store in DATA

SHIFT REGISTER 310); determining if said state of said second element (DR9) is equal to said second expected state (via 389) and generating a second signal (output of 389); and generating a valid output (FAST VERIFY OUTPUT of 390) if both said first and second signals are the same (the XNOR function of 390).

Jones also implies that fuses (or anti-fuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in Jones (see for example column 13, lines 23-26).

Jones does not disclose that the first and second elements are a thin oxide gated fuse having an oxide that is less than 2.5nm thick, and that the state is a state of the electrical resistance.

Gelsomini discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6 and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent, as a fuse).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute a thin oxide gated fuse having an oxide that is less than 2.5nm thick for the first and second memory elements of Jones, as an equivalent memory element, with an optimum oxide thickness, such that the state is a state of the electrical resistance, for the purpose of minimizing the voltage and duration of a programming pulse (as implied in Gelsomini, column 4, lines 2-6), since discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art.

6. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. Pat. No. 5,996,091) in view of Gelsomini et al. (U.S. Pat. No. 6,611,040) as applied to claim 1 above, and further in view of Harshfield (U.S. Pat. No. 5,818,749).

Regarding claim 7, the Jones/Gelsomini combination discloses the method of claim 1, but does not disclose that determining the state of the element includes determining states of first and second thin oxide gated fuses.

Harshfield discloses determining the state of an element includes determining the states of first and second fuses (as complementary pair of fuses in columns C1 and C'1, in Fig. 10).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to have a complementary pair of fuse for the memory element of Jones (using a differential sense amplifier to determine the state of the memory element, as in Harshfield), since use of complementary pair of memory elements was common and well known in the art, for the purpose of improving the integrity of stored data and ensuring the storage of a desired logic state (see for example Harshfield, column 9, lines 21-29).

7. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. Pat. No. 5,996,091) in view of Gelsomini et al. (U.S. Pat. No. 6,611,040) as applied to claim 1 above, and further in view of Giolma (U.S. Pat. No. 5,384,746).

Regarding claims 15 and 16, the Jones/Gelsomini combination discloses the method of claim 9, with the exception of comparing mirroring reference and fuse currents, or at least one current amplifier qualified by a data input. Giolma discloses a means for comparing mirroring reference and fuse currents (12 in Fig. 1 and column 3, line 17 through column 4, line 25), or at

least one current amplifier qualified by a data input (within 12). It would have been obvious at the time the invention was made to a person having ordinary skill in the art to incorporate Giolma's means for comparing the mirroring and reference currents, or at least one current amplifier qualified by a data input, in the method of the Jones/Gelsomini combination, for the purpose of preventing a false reading of a data fuse (Giolma, column 1, lines 66-68).

8. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jones et al. (U.S. Pat. No. 5,996,091) in view of Gelsomini et al. (U.S. Pat. No. 6,611,040) and Khoury (U.S. Pat. Appl. Pub. No. 2003/0011379).

Regarding claim 20, Jones, for example in Figs. 3a and 3b, discloses a memory device comprising: at least one memory cell (within 304 in Fig. 3a); at least one verify circuit (308) connected to said memory cell; sensing a state of said at least one memory cell (to store in DATA SHIFT REGISTER 310); at least one exclusive nor gate (390) connected to said verify circuit; and a logic gate (380) connected to said exclusive nor gate generating a valid signal (FAST VERIFY OUTPUT OF 390 in Fig. 3b).

Jones also implies that fuses (or anti-fuses), flash cells and SRAM cells are equivalent elements for the memory disclosed in Jones (see for example column 13, lines 23-26).

Jones does not disclose at least one reference cell; and that the at least one memory cell has at least one thin oxide gated fuse having an oxide that is less than 2.5nm thick, and that the state is a state of the electrical resistance.

Gelsomini discloses a thin oxide gated fuse (as described in paragraph 50 of the instant application) having an oxide that is less than 2.5nm thick (see for example column 4, lines 2-6

and claim 5), wherein a state of the fuse is a state of the electrical resistance of the fuse (inherent, as a fuse) and sensing a state of such element (via a sense amplifier S/A 132 in Fig. 1).

Khoury discloses a reference cell (34 in Fig. 2).

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to substitute a thin oxide gated fuse having an oxide that is less than 2.5nm thick for the at least one memory cell of Jones, as an equivalent memory element, with an optimum oxide thickness, such that the state is a state of the electrical resistance, for the purpose of minimizing the voltage and duration of a programming pulse (as implied in Gelsomini, column 4, lines 2-6), since discovering an optimum value of a result effective variable (the oxide thickness) involves only routine skill in the art.

Further, it would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a reference cell in the device of the Jones, since use of a reference cell to determine/sense the state of a memory cell, as in Khoury, was common and well known in the art.

Double Patenting

9. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

10. Claims 1, 4-10, 13, 14 and 17 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-5 of U.S. Patent No. 6,704,236.

Although the conflicting claims are not identical, they are not patentably distinct from each other because:

Regarding claims 1, 4, 7-9, 13, 14 and 17 of the instant application, claims 1-5 of Patent recite a method of verifying a state of an element comprising: determining if the state of the element is equal to an expected state (claim 4 of Patent) using a verify circuit (for the method for verifying), wherein a state of the element is a state of the electrical resistance of the element (inherent, as a fuse); and outputting a valid signal if the state of the element is equal to said expected state (claims 1 and 4 of Patent), wherein the element comprises a thin oxide gated fuse having an oxide that is less than 2.5nm thick (claims 3 and 5 of Patent); and further including sensing the state of the element (claim 4 of Patent); determining if the state of first and second thin oxide gated fuses is equal to a first and second expected states and generating first and second signals (claims 1 and 4 of Patent).

Regarding claims 5, 6 and 10 of the instant application, claims 1-5 of Patent recite a method as in claim 1 or 9, with the exception of generating a high/low signal if the state of the

element is equal/not equal to said expected state, or outputting a valid signal if both said first and second signals are high. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to generate a high/low signal if the state of the element is equal/not equal to said expected state, or output a valid signal if both said first and second signals are high, since such designation of a logic state to indicate the result of a condition requires only routine skill in the art.

Response to Arguments

11. Applicant's arguments filed 09 January 2008 have been fully considered but they are not persuasive.

Regarding claims 1, 9, 17 and 20, Applicant argues, on pages 5 and 6, that Jones does not teach the amended limitations, and more specifically, near the bottom of page 5, that the "exclusive OR (XOR) gate 380" of Jones does not compare or determine "electrical resistance".

In response, as indicated in the rejections above, the state of a fuse is inherently determined by its electrical resistance (including the logic states of a high resistance state and a low resistance state). Therefore, in the combination of Jones and Gelsomini, the verify circuit of Jones would determine the state of the electrical resistance of the fuse.

Regarding the previous double patenting rejection, Applicant indicated, at the bottom of page 8, that "Assignee presents Examiner with a terminal disclaimer." However, said terminal disclaimer is not found in the record as having been filed. Therefore, the double patenting rejection has been maintained above.

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to J. H. Hur whose telephone number is (571)272-1870. The examiner can normally be reached on M-F 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

jhh

/J. H. Hur/
Primary Examiner
Art Unit 2824
04 February 2008